CLAIMS

What is claimed is:

Sub A17

1. A system comprising:

clock recovery circuitry to receive a data signal and a reference clock signal and in response thereto to produce an in phase clock signal which is in phase with the data signal and mirrors frequency changes in the data signal, wherein the data signal has embedded clock information and a varying frequency; and

a receiving gate to receive the data signal and the in phase clock signal and to gate the data signal to produce a gated data signal in response to the in phase clock signal.

2. The system of claim 1, wherein the clock recovery circuitry includes:

a phase detector to receive the data signal and in response thereto to produce a phase information signal,

mirroring circuitry to receive the data signal and the reference clock signal and in response thereto to produce a frequency mirrored clock signal that mirrors frequency changes in the data signal,

a phase interpolator to receive the phase information signal and the frequency mirrored clock signal and in response thereto to produce the in phase clock signal.

3. The system of claim 2, wherein the mirroring circuitry includes demodulator circuitry to create a signal representative of frequency changes in the data signal.

4. The system of claim 3, wherein the mirroring circuitry includes an RF mixer to frequency modulate the reference clock signal and the signal representative of frequency changes in the data signal.

5. The system of claim 3, wherein the demodulator circuitry includes histogram analysis.

6. The system of claim 1, wherein the mirroring circuitry includes an RF mixer to frequency modulate the reference clock signal and a signal representative of frequency changes in the data signal.

7. The system of claim 1, further comprising a local reference source to produce the reference clock signal, wherein the reference clock signal has a constant frequency.

8. The system of claim 1, further comprising:

a transmitting chip including a transmitter to produce the data signal to an interconnect in response to a SSC transmitting clock signal; and

a receiving chip coupled to the transmitting chip through the interconnect, the receiving chip including the clock recovery circuitry and the receiving gate.

9. The system of claim 8, further comprising a local reference source external to the receiving chip to produce the reference clock signal, wherein the reference clock signal has a constant frequency.

10. The system of claim 8, wherein the system is included in a computer system.

11. The system of claim 8, wherein the system is included in a communication system.

12. A system comprising:

a receiving gate to receive a data signal and an in phase clock signal and to gate the data signal to produce a gated data signal in response to the in phase clock signal, wherein the data signal has embedded clock information and a varying frequency; and

clock recovery circuitry to receive the gated data signal and a reference clock signal and in response thereto to produce the in phase clock signal which is in phase with the data signal and mirrors frequency changes in the data signal.

13. The system of claim 12, wherein the clock recovery circuitry includes:

a phase detector to receive the gated data signal and in response thereto to produce a phase information signal,

mirroring circuitry to receive the gated data signal and the reference clock signal and in response thereto to produce a frequency mirrored clock signal that mirrors frequency changes in the data signal,

a phase interpolator to receive the phase information signal and the frequency mirrored clock signal and in response thereto to produce the in phase clock signal.

14. The system of claim 13, wherein the mirroring circuitry includes demodulator circuitry to create a signal representative of frequency changes in the data signal.

15. The system of claim 14, wherein the mirroring circuitry includes an RF mixer to frequency modulate the reference clock signal and the signal representative of frequency changes in the data signal.

16. The system of claim 14, wherein the demodulator circuitry includes histogram analysis.

17. The system of claim 12, wherein the mirroring circuitry includes an RF mixer to frequency modulate the reference clock signal and a signal representative of frequency changes in the data signal.

18. The system of claim 12, further comprising:

a transmitting chip including a transmitter to produce the data signal to an interconnect in response to a SSC transmitting clock signal; and

a receiving chip coupled to the transmitting chip through the interconnect, the receiving chip including the clock recovery circuitry and the receiving gate.

19. A system comprising:

clock recovery circuitry to receive a data signal and in response thereto to produce an in phase clock signal which is in phase with the data signal and mirrors frequency changes in the data signal, wherein the data signal has embedded clock information and a varying frequency; and

a receiving gate to receive the data signal and the in phase clock signal and to gate the data signal to produce a gated data signal in response to the in phase clock signal.

20 The system of claim 19, wherein the clock recovery circuitry includes:

a phase detector to receive the data signal and in response thereto to produce a phase information signal,

mirroring circuitry to receive the data signal and in response thereto to produce a frequency mirrored clock signal that mirrors frequency changes in the data signal,

a phase interpolator to receive the phase information signal and the frequency mirrored clock signal and in response thereto to produce the in phase clock signal.

21. The system of claim 20, wherein the mirroring circuitry includes demodulator circuitry to create a signal representative of frequency changes in the data signal.

22. The system of claim 19, further comprising:

a transmitting chip including a transmitter to produce the data signal to an interconnect in response to a SSC transmitting clock signal; and

a receiving chip coupled to the transmitting chip through the interconnect, the receiving chip including the clock recovery circuitry and the receiving gate.

23. A system comprising:

a receiving gate to receive a data signal and an in phase clock signal and to gate the data signal to produce a gated data signal in response to the in phase clock signal, wherein the data signal has embedded clock information and a varying frequency; and

clock recovery circuitry to receive the gated data signal and in response thereto to produce the in phase clock signal which is in phase with the data signal and mirrors frequency changes in the data signal.

24 The system of claim 23, wherein the clock recovery circuitry includes:

a phase detector to receive the data signal and in response thereto to produce a phase information signal,

mirroring circuitry to receive the data signal and in response thereto to produce a frequency mirrored clock signal that mirrors frequency changes in the data signal,

a phase interpolator to receive the phase information signal and the frequency mirrored clock signal and in response thereto to produce the in phase clock signal.

25. The system of claim 24, wherein the mirroring circuitry includes demodulator circuitry to create a signal representative of frequency changes in the data signal.

26. The system of claim 23, further comprising:

a transmitting chip including a transmitter to produce the data signal to an interconnect in response to a SSC transmitting clock signal; and

a receiving chip coupled to the transmitting chip through the interconnect, the receiving chip including the clock recovery circuitry and the receiving gate.